Control of the Unintentional Doping in Epitaxial Graphene FETs

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The transport properties of graphene with saturation currents as high as 2.0 A/mm and electron mobilities of 15 000 cm^2/Vs [1] place this material in the limelight as an attractive candidate of next-generation nanoelectronic devices. The widely observed high carrier mobility naturally focuses our attention towards high frequency performance of graphene based devices. Gigahertz operation of exfoliated [2] and epitaxial [3] graphene FETs has been reported showing cut-off frequency up to 170 GHz [4]. A common trend [3] for these top gated epitaxial graphene FETs that they are highly n-type doped so switching them off is a difficulty. While it is not necessary a problem for analog applications, graphene could offer mixed analog/digital integration with an ease, and for digital transistors a low leakage off state is a necessity. For that purpose devices with close to intrinsic doping have to be fabricated. Here we present the study of the effect of different high-κ oxides and gate metals on the doping level of epitaxially grown graphene on SiC substrates.

Epitaxial graphene was grown on Si-face 6H-SiC. The epitaxial film may consist of double layer parts especially where the underlying SiC substrate has steps. According to AFM characterization and Raman measurements the graphene thickness is 1-2 layers in average over the wafer. A recent study has shown [5] that while double-layer graphene may be present in the immediate vicinity of the steps, it represents only a small perturbation to the normal linear dispersion relationship expected for single-layer graphene. To form FETs we patterned the graphene by e-beam lithography using HSQ and etched it in O_2 plasma. In terms of the gate oxide we fabricated two samples for comparison one with ~20 nm spin-on HSQ and another without it. Both got a 20 nm thick atomic-layer-deposited Al_2O_3 film. E-beam evaporated Cr/Au contacts were lastly deposited to form field-effect transistors (FETs). Hall measurements reveal $\mu \sim 500 - 600$ cm^2/Vs throughout the sample, showing smooth variation and better performance in the middle of the wafer. The DC output characteristics of the devices were linear up to 5 V and slightly sub-linear at higher biases. The drain current had relatively weak (~ 1.5x - 3x) gate dependence as we swept the gate voltage between +/- 10 V. We performed a broader study to characterize the effect of the oxides and for that we used a more simple structure: 1x1 cm samples with metal contacts in the corners. Our conjecture was that a component of the high n-type doping are the states on the graphene/oxide interface. To test this we tried several materials (SiO2, HSQ, Al2O3, HfO2) deposited by different methods (e-beam evaporation, ALD, spin-coat). Another reason for the doping can be the polar nature of the oxide, what we tested by deposited a second layer of highly polar oxide after the surface layer.

We find that all the tested oxides introduced n-type doping. The quantity of the doping shows correlation to the dielectric constant of the oxides. By removing the oxide the initial doping can be restored. In case if we deposited a high-κ oxide on the top of the low-k oxide the n-type doping increased further. High temperature annealing can increase crystallinity of the oxide therefore decrease trapped charge density. We experienced some improvement in case of 600 °C rapid thermal annealing (RTA) but the quick thermal expansion introduced cracks in the oxide.

Our experiment showed that the unwanted doping effect can be minimized by utilizing certain oxide stacks, but intrinsic or p-type doping was not achieved. Growing on lightly p-doped SiC wafer or the use of a polymer surface layer can be a solution and it will be the subject of our further investigation.

References

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Figures

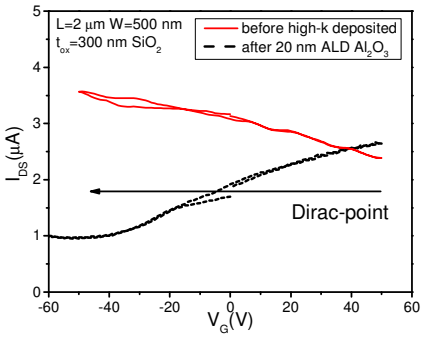


Figure 1. Doping effect of the high-κ top gate dielectric deposition in case of an exfoliated graphene FET on SiO_2. The FET has heavy p-type doping before high-κ deposition, the Dirac point is at some voltage higher than +50 V. After 20 nm ALD Al2O3 deposition the position of the Dirac point decreased by more than 100 V. It corresponds to more than $-7\cdot10^{12}$ cm^{-2} change in the carrier concentration at a given bias.

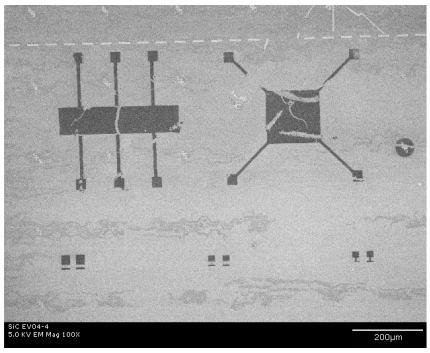


Figure 2. SEM micrograph of graphene on SiC. The cracks on the graphene are caused by the 600 °C rapid thermal annealing of the HSQ mask. Even though RTA can be beneficial to handle the unintentional doping of graphene the structural failure of the oxide excludes it as a useful tool in processing.

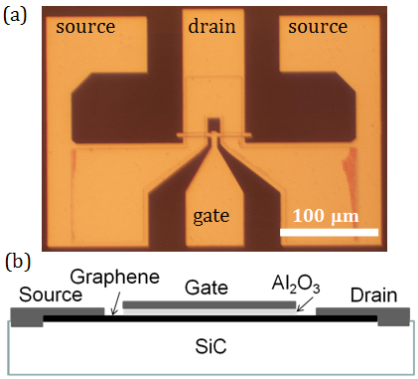
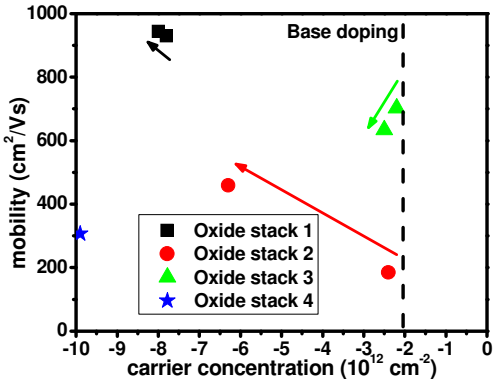
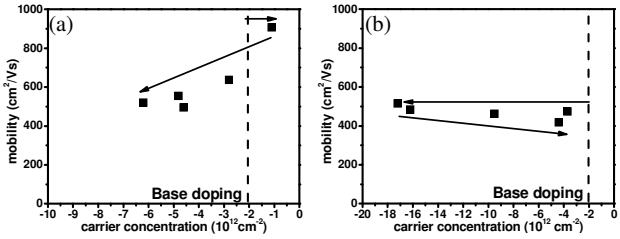


Figure 3. Optical image (a) and schematic cross-section (b) of a processed graphene FET on SiC optimized for RF amplification.



	R_s (kOhm/□	µ (cm^2/Vs)	doping (10^{12} cm^{-2})
Base value	1.0	1040	-2.1
Oxide stack 1			
5 nm ebeam evaporated	0.86	930	-7.8
+10 nm ALD Al_2O_3	0.82	944	-8
Oxide stack 2			
5 nm ebeam evaporated	13.7	185	-2.4
+10 nm ALD Al_2O_3	2.1	459	-6.3
Oxide stack 3			
HSQ coating (not exposed)	3.9	702	-2.2
+10 nm ALD Al_2O_3	3.9	634	-2.5
Oxide stack 4			
HMDS		N/A	
+ 5 nm ALD Al_2O_3	2.0	307	-9.9

Figure 4. Change of the carrier concentration in case of different oxide stacks. The dashed line shows the initial doping of the sample. None of them provide lower n-type doping concentration than the original doping of the sample. Further high-κ oxide deposition added extra doping. The table shows the data in detail corresponding to the different oxide stacks.



(a)	R_s (kOhm/□)	µ (cm^2/Vs)	doping (10^{12} cm^{-2})
HSQ coating (not exposed)	6.2	907	-1.1
+20 nm ALD Al_2O_3	3.4	636	-2.8
RTA, 400 °C, 1 min	2.3	555	-4.8
RTA, 500 °C, 1 min	1.9	520	-6.2
RTA, 600 °C, 1 min	2.7	495	-4.6

(b)	R_s (kOhm/□)	µ (cm^2/Vs)	doping (10^{12} cm^{-2})
HSQ coating (not exposed)	3.5	474	-3.7
+20 nm ALD HfO_2	0.7	515	-17.2
RTA, 400 °C, 1 min	0.8	483	-16.2
RTA, 500 °C, 1 min	1.4	462	-9.5
RTA, 600 °C, 1 min	3.3	418	-4.4

Figure 5. Change of the carrier concentration in case of HSQ + high-κ oxide stacks and the effect of RTA. The dashed line shows the initial doping of the sample. (a) HSQ + Al_2O_3 oxide stack. The RTA continuously increases the doping. (b) HSQ + HfO_2 oxide stack. The highly polar HfO_2 heavily increases the n-type doping but the RTA continuously decreases it. The tables are showing the details of the process.